Understanding Power MOSFET Avalanche Operation and Associated UIS (UIL) Data Sheet Ratings

AND90158/D

In the off state, a power MOSFET's body diode structure is designed to block a minimum drain to source voltage value. The breakdown, or avalanche, of the MOSFET body diode indicates the electric field across the reverse biased body diode is such that significant current flows between drain and source terminals. Typical blocking state leakage currents are on the order of tens of picoamperes to hundreds of nanoamperes. In avalanche, MOSFET drain, or source, currents range from microamperes to hundreds of amperes depending on circuit conditions. The breakdown, or "BV", rating is typically the minimum blocking voltage for the MOSFET device (e.g., 30 V) defined over a given temperature range (often the full operating junction temperature range). The data sheet BVdss value is the device avalanche voltage measured at a low avalanche current, typically 250 μA or 1 mA, and at junction temperature = 25°C. BVdss data over a junction temperature range, or BVdss temperature coefficient value, is often provided on data sheet as well. This is important to note as power MOSFET avalanche voltage is strong function of both junction temperature and avalanche current. Figure 1 shows BVdss values for three temperatures as a function of avalanche current for a 30 V rated device. Table 1 below lists range of typical avalanche voltage ranges for different power MOSFET BV ratings–measured at high avalanche current (amperes) and elevated junction temperatures (at or near maximum rated junction temperature).

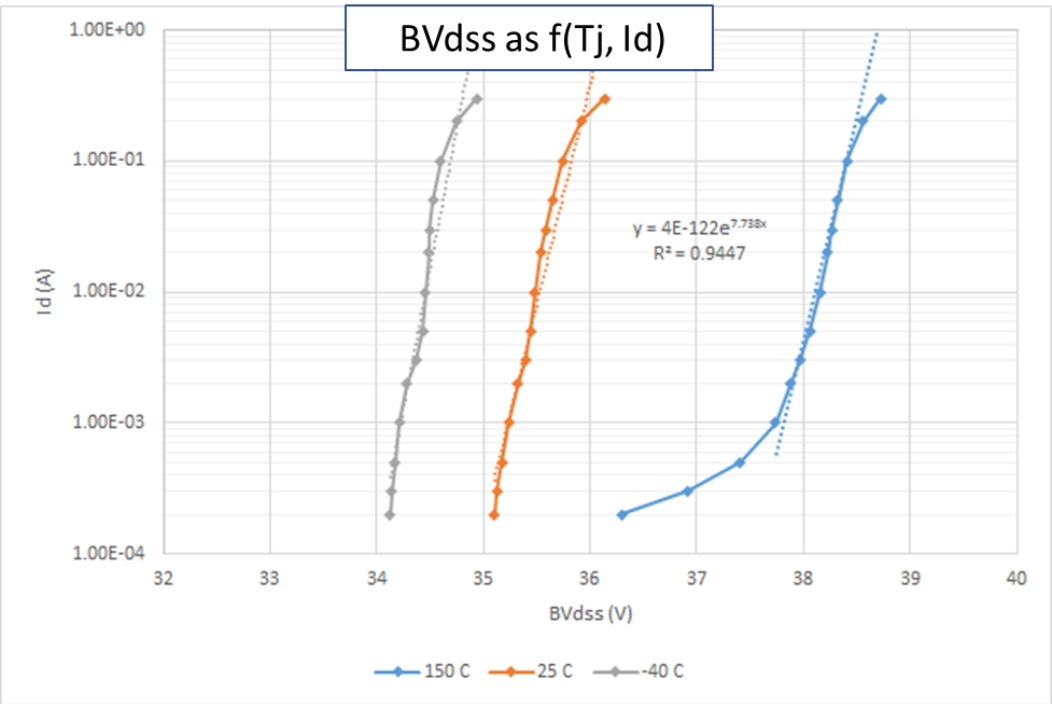

Figure 1. Avalanche Voltage as Function of Junction Temperature and Avalanche Current for a 30 V Rated MOSFET Device

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Table 1. Typical Ranges of Avalanche Voltages at High Tj and High Iav Conditions for Different BV Classes

Rated DV (V)	Vav (V)
30	44–47
40	55–59
60	85–90
80	115–120
100	140–150

The power function (avalanche voltage * avalanche current) of a MOSFET operating in avalanche can be of any form. This application note covers a specific avalanche power function that forms the basis of avalanche ratings found on power MOSFET data sheets. MOSFET data sheets typically specify avalanche ratings under the synonymous terms “UIS” or “UIL” meaning “Unclamped Inductive Switch–off” or “Unclamped Inductive Load”. That is, power MOSFET avalanche ratings apply to the resultant Vds and Id (these terms assume an n–channel MOSFET, otherwise Vsd and Is for p–channel MOSFET) waveforms when a MOSFET driving an unclamped load is switched off. Figure 2 shows the basic circuit and Figure 3 shows device waveforms. Going forward we continue to assume a n–channel MOSFET and define terms as:

Iav = avalanche current

Ipk = maximum avalanche current= value when MOSFET is switched off

Ipk (fail) = maximum avalanche current when MOSFET fails (drain to source to gate short)

Jpk, Jpk (fail): Ipk value scaled to die active area, in units A/area^2

Die active area: area of MOSFET die containing active MOSFET structures; some percentage of total die area

Vav = avalanche voltage (Vds). Vav is often not constant during avalanche (since Iav and Tj change); Vav is usually the average Vds magnitude measured during time in avalanche

tav = time in avalanche, typically defined as the time required for Iav to decrease from Ipk to zero; that is the time for the energy stored in the inductor to decrease to zero.

Tj = MOSFFET junction temperature, often simply noted as the maximum temperature on or near die surface.

Tj (intrinsic) = MOSFET junction temperature where device junction becomes a conductor (thermally generated carriers swamp dopant carriers); at this temperature the MOSFET typically fails with characteristic of permanent drain to source to gate short.

energy (E, or sometimes listed as Eav or Eas) = the time integral of the avalanche power function; for a pure triangular function in avalanche, E = 1/2 *Vav*Ipk*tav

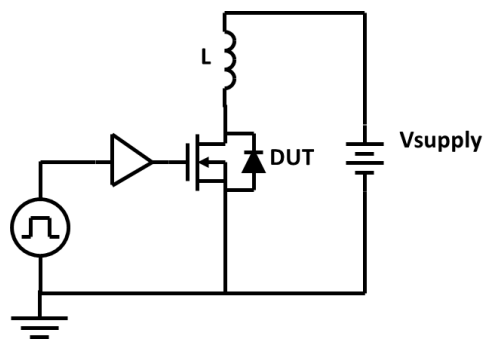

Figure 2. Basic Unclamped Inductive Switch Off Circuit. DUT (Device Under Test) is Power MOSFET Device. Triangle Form Represents Gate Drive Circuit.

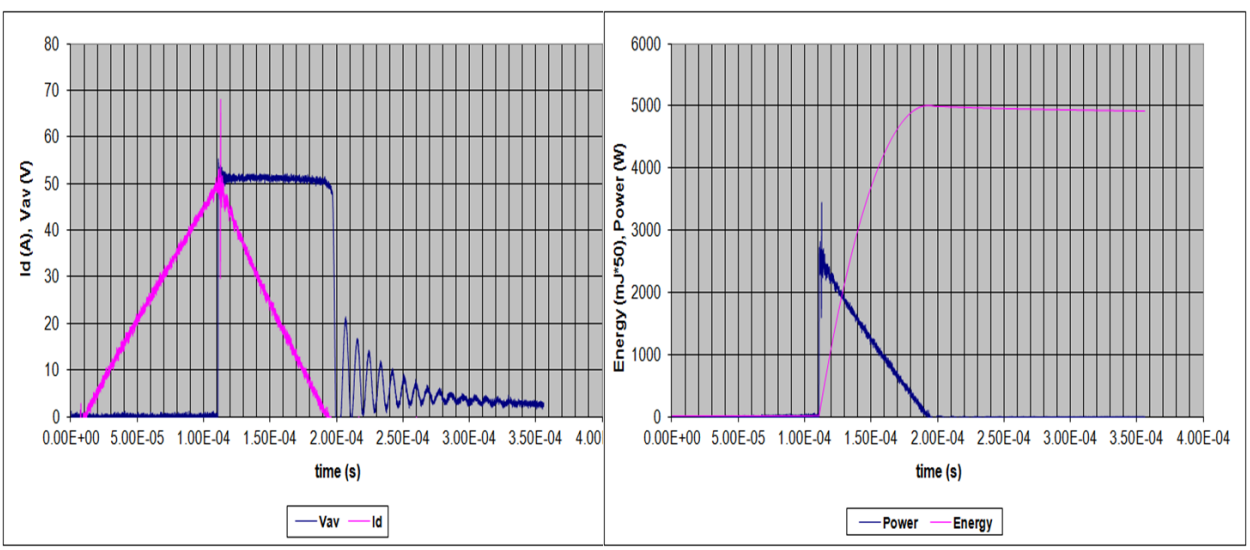

Figure 3. Unclamped Inductive Switch–off Waveforms for MOSFET DUT. Energy Function is the Integral of the Power Function.

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Power MOSFETs configured in high−side configuration (see Figure 4) can avalanche, depending on gate drive conditions. If the gate driver at switch−off brings the gate and source potentials together so that Vgs << Vth, then the source potential can drop to the necessary negative value for the device to avalanche. However, if the gate drive at switch−off brings the gate potential to zero, the source potential can decrease to a negative value only to the point where the device turns back on. That is, Vgs becomes positive and reaches the value necessary for avalanche current to flow while the device is in saturation (typically slightly greater than Vth, depending on Iav magnitude and device gain). In this case the MOSFET is operating in saturation during the time in clamp (as the inductor stored energy decreases to zero). This "self−active" clamp operation mode affords a potential issue, thermal runaway, a subject not covered in this application note.

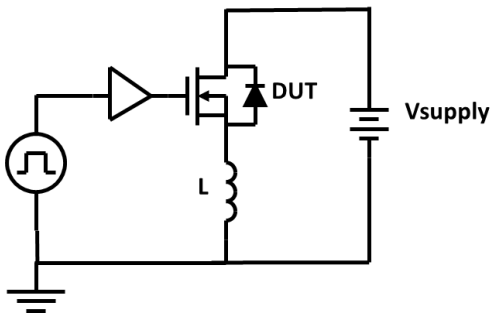

Figure 4. Basic High−side Configured Unclamped Inductive Load Switch−off Circuit

Most applications do not switch−off MOSFETs to unclamped loads by design. However, there are some applications that by design do switch unclamped inductive loads. Examples include some fuel injection systems, ABS dump coils, and low cost, low power solenoid loads where cost of clamping diode can be eliminated. More often, application avalanche issues and possible resultant device failures result from switch−off of unclamped stray inductances of PCB traces and cable wiring, ESL of resistors and capacitors, and package interconnect inductance of transistors and diodes. Examples include switch−off from short circuit faults (often very high Ipk and low tav), and switch node overshoot in converter and inverter topologies. Avalanche events on MOSFETs can also result from transients on the supply line (for example alternator load dump); avalanche operation does not necessarily require switch−off of unclamped inductive loads. However, UIS (UIL) data found in power MOSFET data sheets can often be useful to evaluate these avalanche events, depending on the composition of the avalanche power function.

In general, MOSFET UIS capability is determined by subjecting device samples to avalanche pulses until failure. Most often, a fixed inductor value is selected and peak current thru the inductor is incremented until the DUT (device under test) fails (characterized by a drain to source to gate short). Sufficient time is allowed between each Ipk increment to ensure the DUT junction temperature returns to initial conditions prior to next avalanche pulse. Initial junction temperature is controlled either by oven, forced air, or heater block. Generally, UIS data is collected at Tj(initial) = 25°C, and at least one elevated initial junction temperature (e.g., 100°C). The test circuit can be configured so that the DUT is either used to ramp current the inductor load or connected as diode (Vgs= 0 V) and a higher avalanche switch is used to ramp and switch−off inductor current. Compare the circuits in Figure 5. There are two potential issues to consider when using the DUT as the MOSFET switch to ramp current into the conductor. First, during the time the current increases to Ipk the MOSFET DUT is dissipating power (typically = I^2*Rds(on)) so the device can self−heat thereby increasing Tj(initial) at switch−off. This can be mitigated by ensuring sufficient Vgs gate voltage to reduce Rds(on) and using as high as possible supply voltage in order to minimize time required to reach Ipk (time from 0 A to Ipk = L*Ipk/Vsupply). The second issue is gate drive sink capability during switch−off. If the device is switched off slowly, some of the stored inductor energy is dissipated in the switching transition. If switched off slowly enough, avalanche can be avoided. In general, power MOSFET data sheet UIS specifications assume a hard switch−off event, ensuring nearly all the inductor stored energy is dissipated by the MOSFET in avalanche operation.

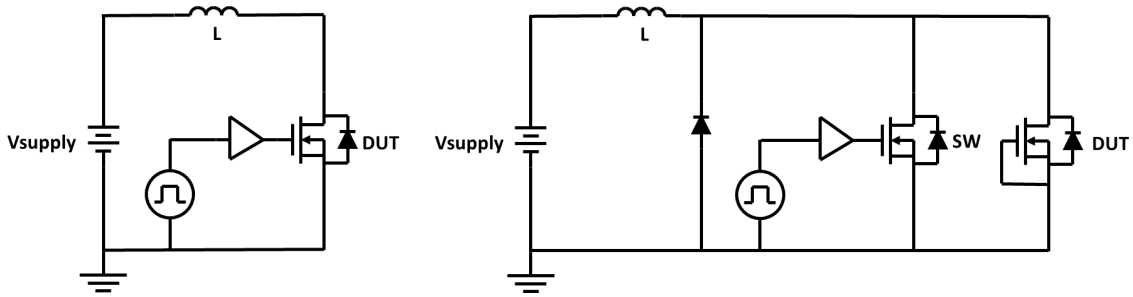

Figure 5. Left Circuit is Basic Self−driven UIS Test Circuit. Right Circuit is Test Circuit where DUT is configured as Diode and Secondary Switch (SW) controls Inductor Current. Vav (SW) >> Vav (DUT).

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The UIS data collected is a set of Ipk(fail) and associated tav operating points for several different inductor values. From this data set, an Ipk(fail) vs tav curve, for a given Tj(initial) is generated (see Figure 6). The data should fit well to a power function of the form $Ipk = A*tav^{-\alpha}$, where A is a constant and the α exponent magnitude is usually on the order of 0.5. This is significant because it indicates a likelihood that the Ipk fail operating points represent thermal based failures. The power function $Ipk = A*tav^{-\alpha}$ can be rewritten as $A^{(1/\alpha)} = Ipk^{(1/\alpha)}*tav$. If $\alpha = 0.5$, we get the result Ipk^2*tav = constant. This is a typical expression for modeling mechanical fuse (those that open due to material reaching melting point) current and time to open (melt) characteristics. In this sense, the power function $Ipk = A*Ipk^{-\alpha}$ can indicate a thermal failure mechanism. The importance and insight regarding power MOSFET UIS capability being a thermal base failure is discussed later.

The Ipk(fail) versus tav data is de−rated to generate the data sheet plot, which may be considered a SOA (safe operating area) for power MOSFET unclamped inductive switch−off avalanche operation (see Figure 7). If the application Ipk and tav operating point is below the Ipk vs tav curve and the initial Tj for the curve, then the device is safe to operate. From a thermal perspective this could be done for any number of avalanche pulses if each pulse begins at a junction temperature state at or below the stated Tj(initial) value. However repetitive avalanche pulses may result in MOSFET parameter shifts due to a HCI (hot carrier injection) mechanism depending on device technology and operating conditions. Repetitive avalanche is discussed later in this application note.

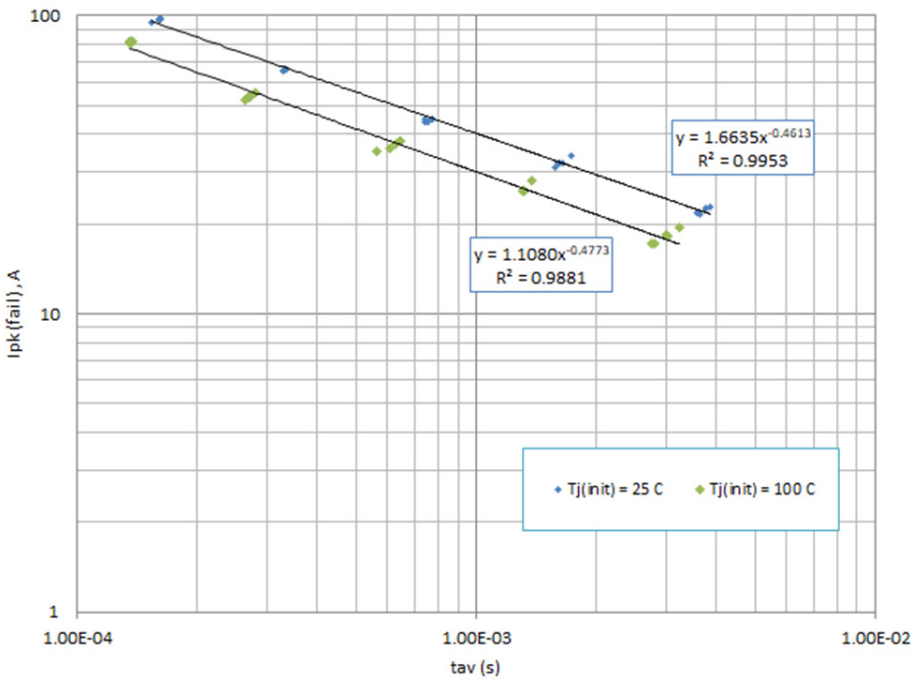

Figure 6. Ipk(fail) Data as Function of Time in Avalanche at Two Initial Junction Temperatures

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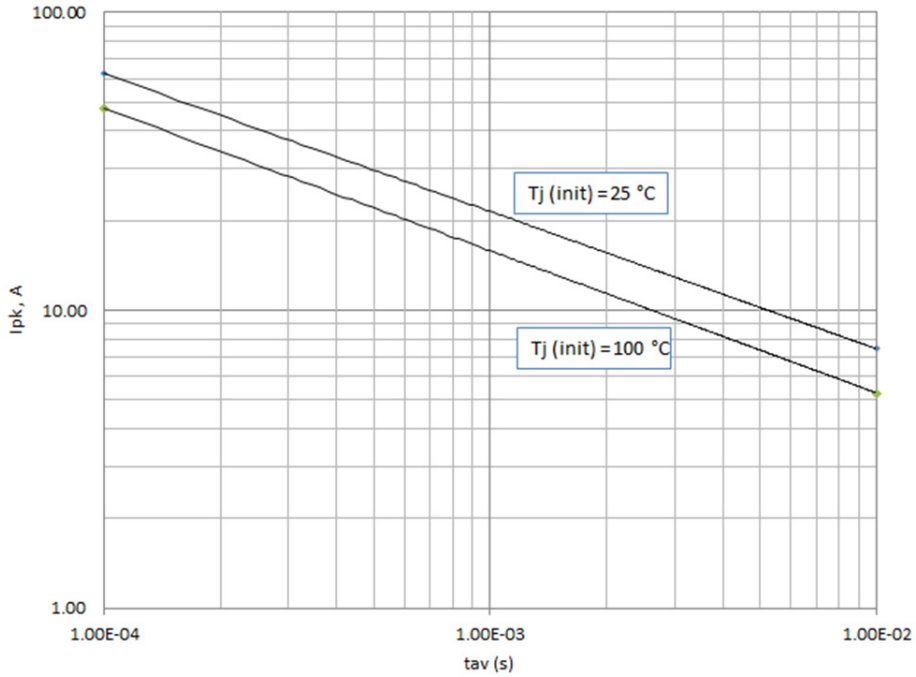

Figure 7. Ipk(fail) vs tav Data of Figure 6 De−rated to Form Data Sheet Ipk vs tav SOA Plot

To de−rate the Ipk(fail) data, the Ipk (fail) value is lowered to some percentage (X) of original value, and tav is adjusted for the new Ipk value for the inductance value used in the measurement of Ipk(fail). Adjusted tav is given by: tav(de−rated) = L*Ipk(fail)*X/Vav. The de−rated Ipk function is given by Ipk = B*tav$^{-\alpha}$, where the new de−rated coefficient, B, can be calculated from: B = A*X*(1/X)$^{-\alpha}$, where X is the de−rating percentage. The X value is generally conservative and may range from approximately 50 % − 75 % across the industry.

In addition to the Ipk vs tav plot, most power MOSFET data sheets include a single UIS energy rating, often listed in the table of maximum values. This is a bit misleading, as it should be obvious (E = 0.5 Vav*Ipk*tav) that a power MOSFET can theoretically have an infinite number of energy ratings, if one measured with an infinitely small inductor (tav approaches zero) and infinitely large inductor (tav approaches infinity). The energy dissipated in UIS avalanche pulse for a power MOSFET increases as tav increases. (see Figure 8). Any single UIS avalanche rating can be taken as any Ipk, tav operating point that lies on the Ipk vs tav SOA curve, for some given Tj(initial) value. Some reasons why one operating point is selected over another for a data sheet “maximum” rating include selection of operating point as the same used to screen the device at end of line test, or for marketing or customer purposes to indicate some desired energy level. The key point, when comparing one device UIS capability to another, is to compare the Ipk vs tav plot data at the same Tj(initial) temperature and *not* compare single UIS rating values.

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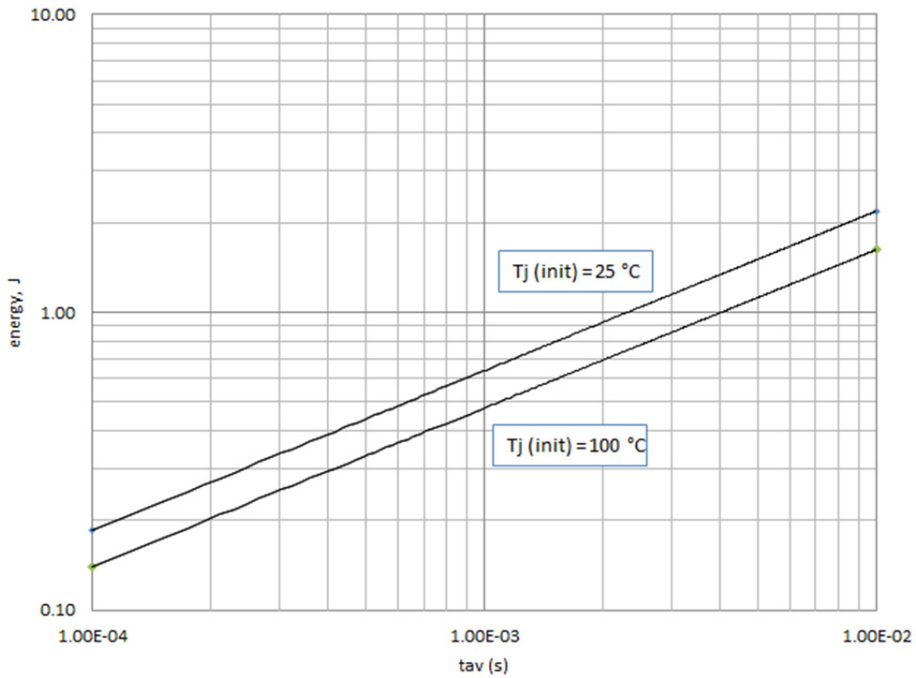

Figure 8. Data from Figure 7 Data Translated to Energy as Function of Time in Avalanche. UIS Energy Increase as tav Increases.

Several design and associated wafer processing attributes are utilized to affect power MOSFET UIS capability. Chief among these is design and processing of the source metal contact (which is discussed later) but discussion of these attributes is not necessary to understand the main goal for any power MOSFET design, regarding UIS capability, is to ensure the device fails thermally. That is the energy dissipated in the device due to avalanche operation is limited only by the thermal capability of the device for that specific power function. MOSFET devices of similar BV characteristics (that is same or similar avalanche voltage) and of similar thermal capability will have similar UIS capability. Since typical UIS avalanche times in real world applications (and listed on data sheet plots) are usually less than one millisecond, and therefore heat flow is not appreciably affected by external thermal boundary conditions; the primary thermal constraint is MOSFET die active area and thickness. Therefore, it is expected that Ipk (fail) capability as a function of tav should scale to die active area within a MOSFET technology and within similar technologies. In fact, this is shown to be true, see Figure 9. The y−axis of Figure 9 is labeled as Jpk(fail), in units of A/mm^2, which is the Ipk(fail) value divided by the device active area for individual MOSFET samples. This affords the ability to include Ipk(fail) vs tav data from any number of different MOSFET samples with different die active areas (in this case ranging from ~ 1 mm^2 to 13 mm^2). Moreover, Figure 9 shows data for three significantly different 60 V MOSFET technologies each with similar avalanche voltage characteristics. It is clear from this data that these different MOSFET technologies with similar avalanche voltage characteristics exhibit the same UIS capability scaled to die active area (or to be more accurate, active die volume). Figure 10 displays Jpk(fail data as a function of time in avalanche for three different sets of data representing three different BV ratings. Figure 10 illustrates that a lower BV rated (lower Vav) device has increased Jpk capability at a given time in avalanche compared to higher BV devices. However, if the data from Figure 10 are plotted in terms of energy (fail) density (in J/mm2), it shows energy density approximately follows the same function regardless of technology and BV rating, further supporting the position that MOSFET UIS capability is scalable to active die active volume (see Figure 11).

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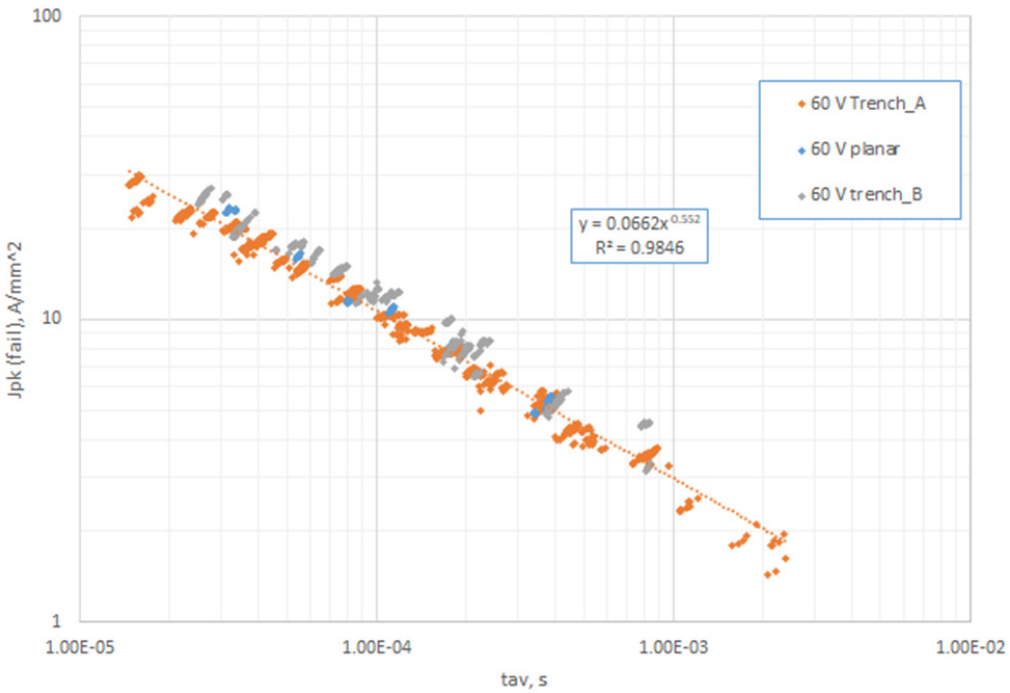

Figure 9. Peak Avalanche Current Density at Failure as Function of tav Data for Three Different 60 V Rated MOSFET Technologies

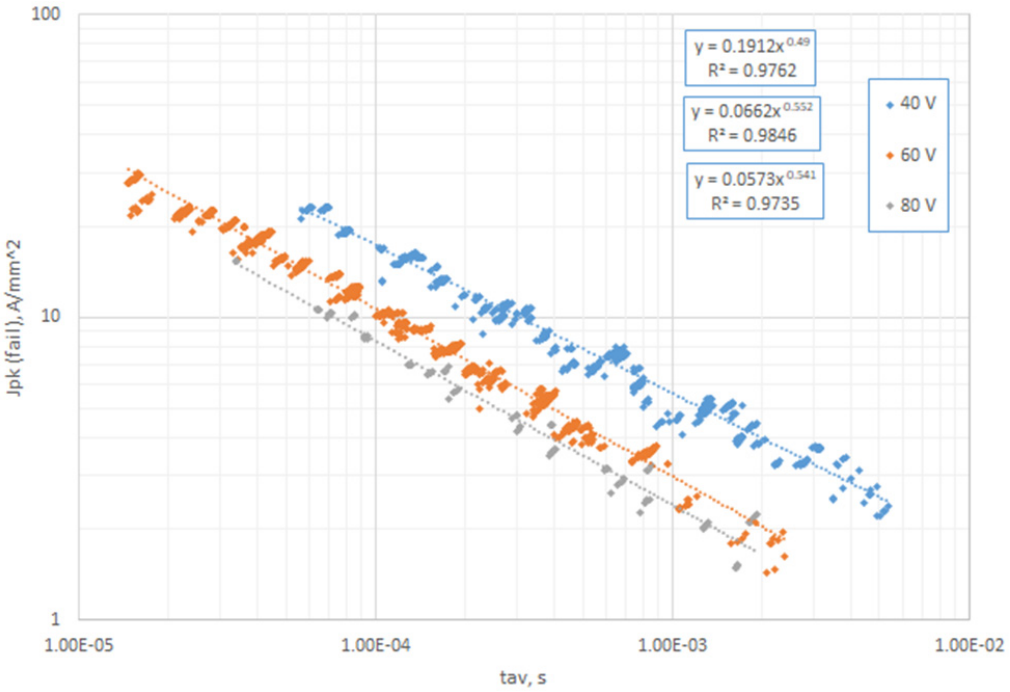

Figure 10. Peak Avalanche Current Density at Fail vs tav Data for Multiple MOSFET Technologies at Three Different BV Ratings

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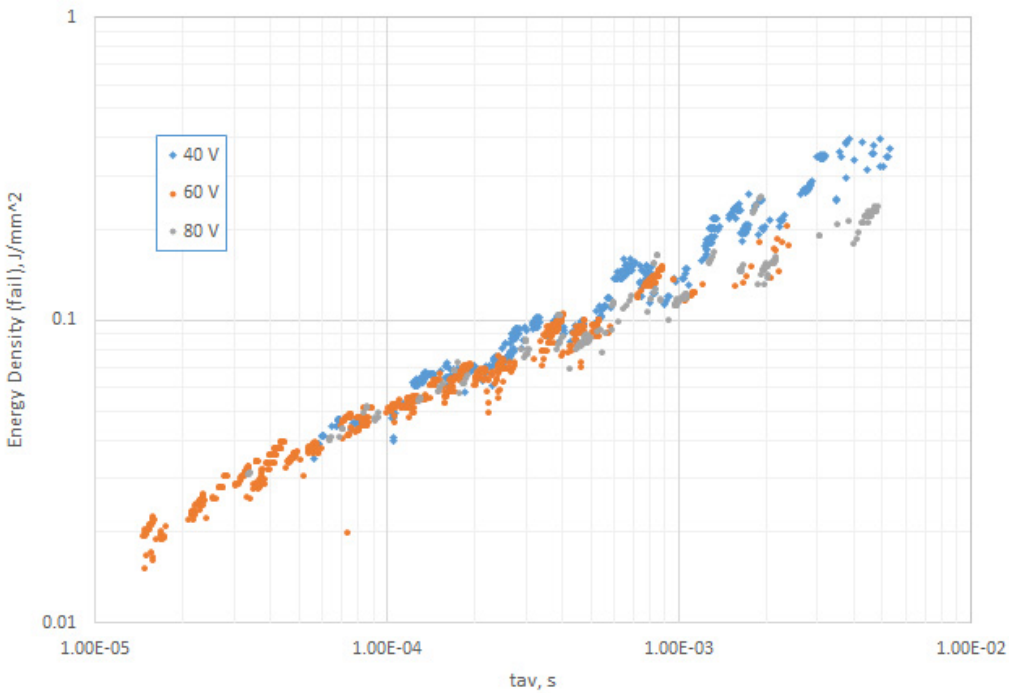

Figure 11. Energy Density at Failure vs tav Data Calculated from Figure 10 Data. This Energy Density Function is approximately the same for any BV Rated Product.

There is an exception to the position that MOSFET UIS capability is limited only by thermal capability of the MOSFET device for any condition. At higher avalanche current densities, the MOSFET device can fail well below an expected thermal based Jpk(fail) value. That is the Ipk vs tav plot on a data sheet cannot be extrapolated ad infinitum to higher Ipk and lower tav values. The reason for this is illustrated in Figure 12. The p-doped region, n−doped source region, and the n−doped drift (epi) region of the MOSFET structure form a npn transistor. The base to emitter junction of this npn transistor, formed by the p−doped region and the n−doped source region is shorted by the front metal. Therefore, the source metal contact is a key design and process parameter for MOSFET UIS capability. If the npn is activated, because the base to emitter is forward biased, significant avalanche current will crowd at the defect site resulting in rapid device failure. The key is to realize that the p−doped region has some resistance level and therefore at some avalanche current density the p−n junction will forward bias so that that npn transistor is activated. Figure 13 shows Jpk(fail) data at low avalanche times compared to greater avalanche times where device Jpk failures are clearly intrinsic thermal based. Thus, any power MOSFET must have a maximum limit to peak avalanche current. This is true even if a data sheet does not list or show a maximum UIS Ipk value. The maximum Ipk limitation in avalanche may be an issue in applications designed to shut−off from very high magnitude short circuit currents. MOSFETs can fail in avalanche at shutoff due to small stray inductance in PCB or supply line wiring even though the avalanche energy is significantly below that necessary for intrinsic thermal failure.

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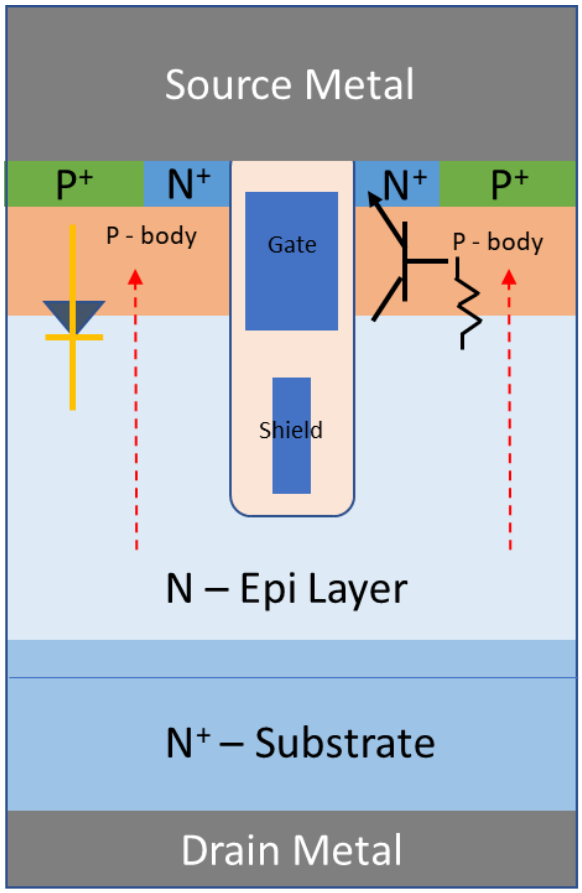

Figure 12. Simplified Cross Section Drawing of Shielded Gate MOSFET Structure showing Internal npn BJT Structure. Dashed Arrows represent Avalanche Current.

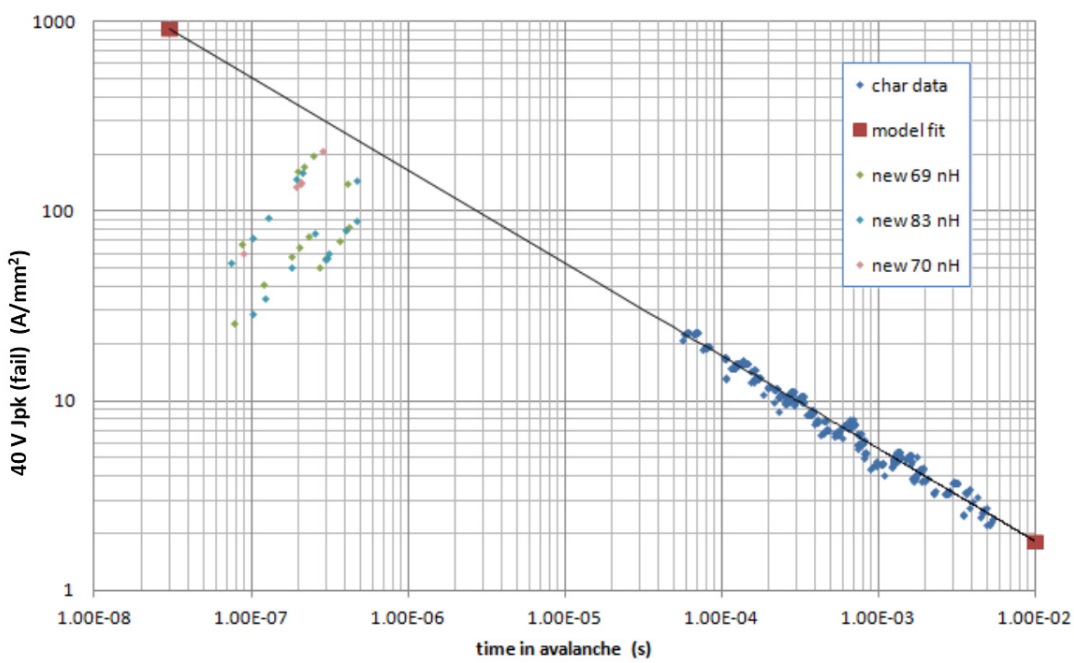

Figure 13. Peak Avalanche Current Density vs. tav for 40 V Rated Product showing Non Thermal Failures at Low Avalanche Times and High Peak Current Density

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A power MOSFET may be operated in avalanche repeatedly, provided each avalanche event is within safe operating limits (Ipk, tav, Tj(initial)). That said, trench based MOSFET technologies (predominate in industry today) can exhibit DC parameter shifts due to repetitive avalanche operation due to an effect akin to hot carrier injection. Figure 14 illustrates this; during avalanche there maybe high current density in the drift (n−epi) region which is under high electric field (the drift or mesa, region is fully depleted). In trench structures the gate and shield oxides are adjacent to the high current avalanche current flow, and the high electric field can knock charge carriers into the gate and shield oxides, depending on operating conditions. This is not the case for planar technology structure during avalanche operation. In general, planar MOSFET structures are immune to repetitive avalanche HCI effects.

The MOSFET DC parameters affected by repetitive avalanche HCI effects include BVdss (avalanche voltage), Idss (off −state drain to source leakage current), Vth (gate to source threshold voltage), and Rds(on) (on−state drain to source resistance). Igss (off−state gate to source leakage current) is not affected by repetitive avalanche operation. Usually, BVdss parameter shift occurs and stabilizes with the first few hundred to thousand repetitive avalanche cycles, but the delta magnitude is typically less than ±3 V, which in most cases does not present an application issue. Idss can increase significantly (from nanoampere range to single microampere range) over millions to hundreds of millions of repetitive avalanche cycles. Mobility in the channel can be affected by repetitive avalanche HCI effects, resulting in Rds(on) increase at the same time Vth decreases, again over millions to hundreds of millions of repetitive avalanche cycles. Whether these parameters change significantly or not and by how much depends on the repetitive avalanche operating conditions (average and peak junction temperature, change in junction temperature, avalanche current density, time in avalanche, and number of avalanche cycles). In general, these parameter shifts do not result in physical device failure, but obviously parameter shifts of the right type, magnitude, and direction can possibly result in end application issues. Figure 15 displays examples of parameter shift data (delta from initial measurement) for trench MOSFET technology device operated in repetitive avalanche conditions.

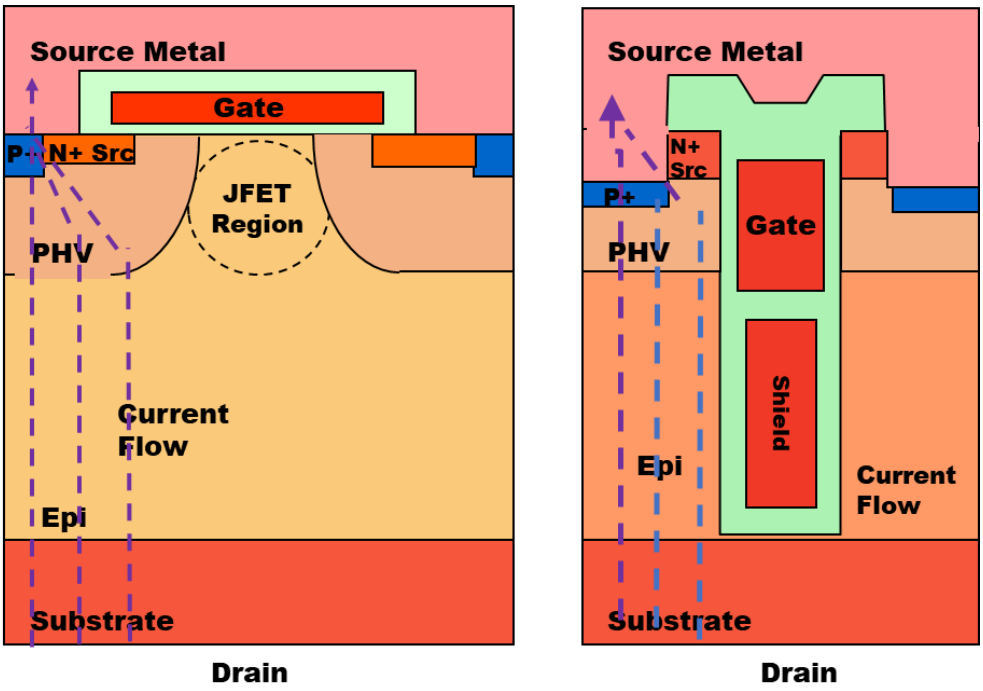

Figure 14. Simplified Cross Section Diagrams of a Planar MOSFET Structure (left) and a Shielded Gate MOSFET Structure (right). Dashed Lines represent Avalanche Current Flow.

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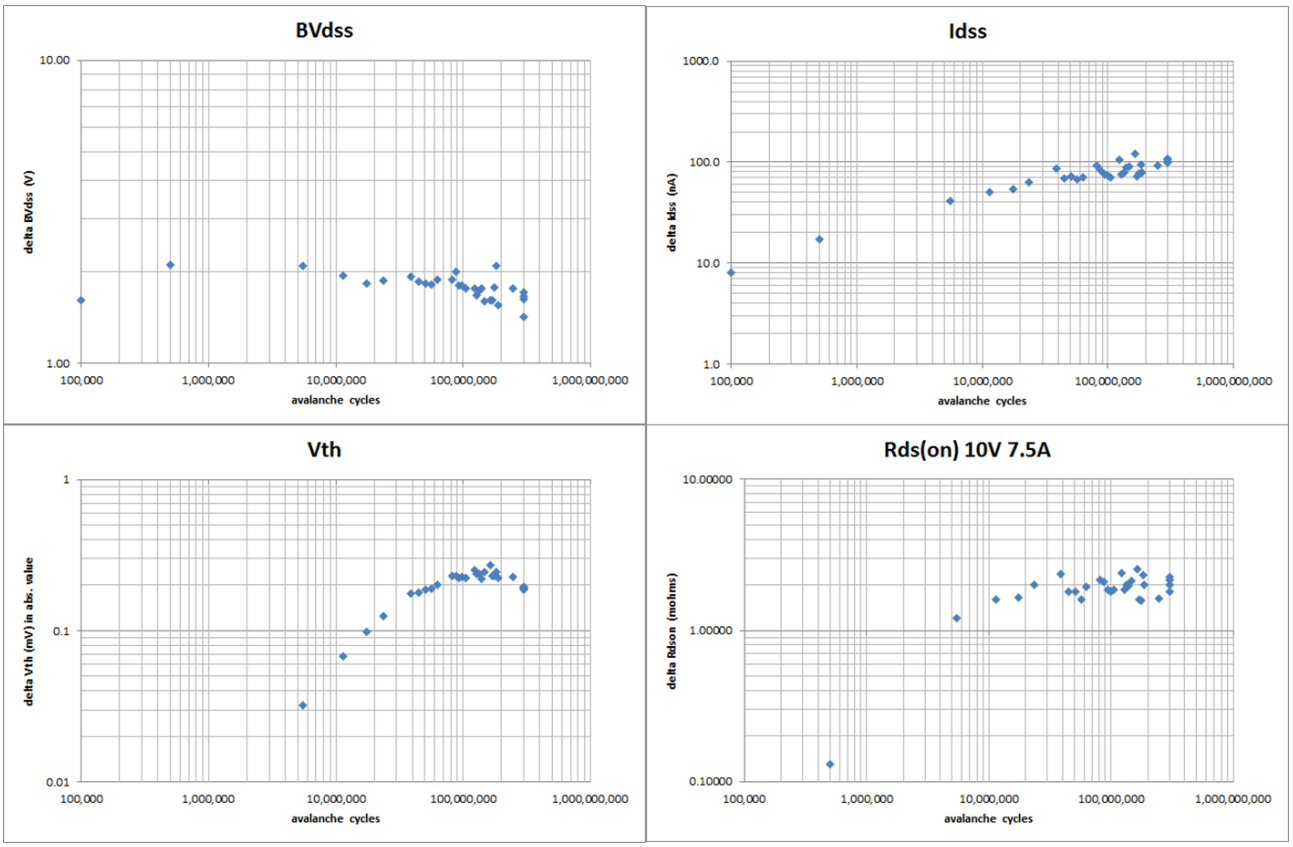

Figure 15. DC Parameter Shift as Function of Repetitive Avalanche Cycles Data for a Trench Technology MOSFET

The key point regarding power MOSFET avalanche operation is there is no defined method to specify power MOSFET repetitive avalanche capability ratings. Any repetitive avalanche rating found on a data sheet should include operating condition assumptions and define the methodology to determine the functional capability limit (e.g., number of cycles to reach some percentage change in some DC parameter). As a general design rule, repetitive avalanche operation should be avoided, as preferred circuit design practice. Of course, this cannot always be practiced; as mentioned earlier in this application note, real world applications exist that require the MOSFET to avalanche repetitively by design. In these cases, determination of a MOSFET suitability to the repetitive avalanche operation is best evaluated empirically, using the application operating conditions.

UIS (UIL) is a specific form of MOSFET avalanche operation, resultant from switch−off of an unclamped inductive load. Power MOSFETs are designed and manufactured so the UIS avalanche operation is limited only by device thermal capability or by maximum peak avalanche current density. Power MOSFET UIS capability is best presented by the Ipk as a function of tav SOA plot. Single UIS energy ratings should not be compared between devices unless test operating conditions (Ipk, Vav, L, tav, and Tj(initial) are known and understood. Devices with same or similar avalanche voltage functions and same or similar thermal capability will have same UIS capability to failure, but de−rating factors for Ipk vs tav SOA plots can vary across industry. Safe repetitive avalanche operation is possible, although DC parameter shifts can occur depending on operating conditions.

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