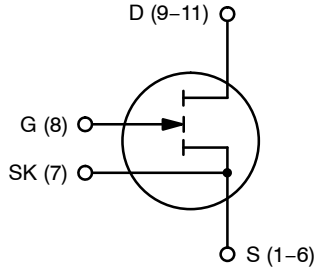
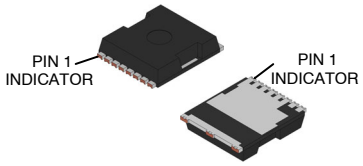
# Enhancement Mode Gallium Nitride (GaN) HEMT

## 650 V, 39 mΩ, 40 A, PDSO-F9

# NTBL050N65GN1

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ TYP | $I_{DS}$ MAX |
|---|---|---|
| 650 V | 39 mΩ | 40 A |




**PDSO-F9 10.38 x 9.90 x 2.30, 1.20P**
**CASE 207AA**

### Features

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Ultra Low Gate Charge for High Speed Switching
- FOM-$Q_G$ = 367 nC*mΩ
- Small Footprint for High Density PCB Design
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

### Typical Applications

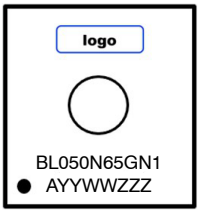
- High Density Power Modules
- High Frequency AC-DC and DC-DC Converters
- High Performance PSU for Datacenter and Industrial
- Resonant Conversion

**MAXIMUM RATINGS** ($T_J$ = 25 °C unless otherwise noted)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain-to-Source Voltage | $V_{DSS}$ | 650 | V |
| Drain-to-Source Transient Voltage, $t_P$ < 200 μs | $V_{DS(TRAN)}$ | 800 | V |
| Gate-to-Source Voltage | $V_{GS}$ | −6 to 7 | V |
| Gate-to-Source Transient Voltage, $t_P$ = 50 ns, $f_P$ = 100 kHz, open drain | $V_{GS(PULSE)}$ | −20 to 10 | V |
| Continuous Drain Current, $T_{CASE}$ = 25 °C<br>$T_{CASE}$ = 100 °C | $I_{DS}$ | 40<br>30 | A |
| Pulsed Drain Current, $t_P$ < 10 μs, $T_J$ = 25 °C<br>$T_J$ = 125 °C | $I_{DS(PULSE)}$ | 77<br>40 | A |
| Power Dissipation, $V_{GS}$ = 6 V, $T_{CASE}$ = 25 °C | $P_{TOT}$ | 250 | W |
| Operating Junction Temperature | $T_J$ | −55 to 150 | °C |
| Storage Temperature | $T_{STG}$ | −55 to 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### MARKING DIAGRAM




| | |
|---|---|
| BL050N65GN1 | = Specific Device Code |
| A | = Assembly Site |
| YY | = Year of Production |
| WW | = Work Week Number |
| ZZZ | = Assembly Lot Number |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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## THERMAL CHARACTERISTICS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction-to-Case | $R_{\theta JC}$ | 0.5 | °C/W |
| Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 56 | °C/W |
| Maximum Soldering Temperature (MSL3) | $T_{SLD}$ | 260 | °C |

1. Device on 1 in$^2$, 2 oz copper pad on single layer FR-4 PCB

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25 °C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V | 650 | | | V |
| Drain-to-Source Leakage Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | 8 | 100 | μA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V, $T_J$ = 125 °C (Note 3) | | 20 | | |
| Gate-to-Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = 6 V, $V_{DS}$ = 0 V | | 250 | | μA |
| | | $V_{GS}$ = 6 V, $V_{DS}$ = 0 V, $T_J$ = 125 °C (Note 3) | | 875 | | μA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| Drain-to-Source On Resistance | $R_{DS(ON)}$ | $V_{GS}$ = 6 V, $I_{DS}$ = 13 A | | 39 | 50 | mΩ |
| | | $V_{GS}$ = 6 V, $I_{DS}$ = 13 A, $T_J$ = 125 °C (Note 3) | | 75 | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 46.8 mA, $T_J$ = 25 °C | 1.2 | 1.5 | 2.5 | V |
| | | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 46.8 mA, $T_J$ = 125 °C (Note 3) | | 1.4 | | |
| **DYNAMIC CHARACTERISTICS** (Note 3) | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, f = 1 MHz | | 338 | | pF |
| Output Capacitance | $C_{OSS}$ | | | 118 | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | 1.5 | | |
| Output Capacitance, Energy Related | $C_{OSS(ER)}$ | $V_{DS}$ = 0 V to 400 V, $V_{GS}$ = 0 V | | 189 | | pF |
| Output Capacitance, Time Related | $C_{OSS(TR)}$ | | | 255 | | |
| Output Charge | $Q_{OSS}$ | | | 102 | | nC |
| Output Capacitance Stored Energy | $E_{OSS}$ | | | 15 | | μJ |
| Gate Resistance | $R_G$ | f = 5 MHz | | 1.5 | | Ω |
| Gate Charge | $Q_G$ | $V_{DS}$ = 400 V, $I_{DS}$ = 13 A, $V_{GS}$ = 0/6 V | | 10.6 | | nC |
| Gate-to-Source Charge | $Q_{GS}$ | | | 4.2 | | |
| Gate-to-Drain Charge | $Q_{GD}$ | | | 1.6 | | |
| Gate Plateau Voltage | $V_{PLAT}$ | | | 2.8 | | V |
| **SWITCHING CHARACTERISTICS** (Note 3) | | | | | | |
| Turn-On Delay Time | $t_{D(ON)}$ | $V_{DS}$ = 400 V, $I_{DS}$ = 13 A, $V_{GS}$ = 0/6 V, $R_{G,ON}$ = 10 Ω, $R_{G,OFF}$ = 4 Ω | | 4.5 | | ns |
| Turn-Off Delay Time | $t_{D(OFF)}$ | | | 9.2 | | ns |
| Turn-On Rise Time | $t_R$ | | | 7.3 | | ns |
| Turn-Off Fall Time | $t_F$ | | | 9.9 | | ns |



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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **REVERSE CONDUCTION CHARACTERISTICS** | | | | | | |
| Source-to-Drain Reverse Voltage | $V_{SD}$ | $V_{GS}$ = –3 V, $I_{SD}$ = 13 A (Note 3) | | 5.4 | | V |
| | | $V_{GS}$ = 0 V, $I_{SD}$ = 13 A | | 2.5 | | |
| | | $V_{GS}$ = 6 V, $I_{SD}$ = 13 A (Note 3) | | 0.5 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. No prior drain bias or switching stress is applied during the measurement of $V_{GS(TH)}$ and $R_{DS(ON)}$.
3. Defined by design, not subject to production test.



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## TYPICAL CHARACTERISTICS ($T_J$ = 25 °C unless otherwise specified)

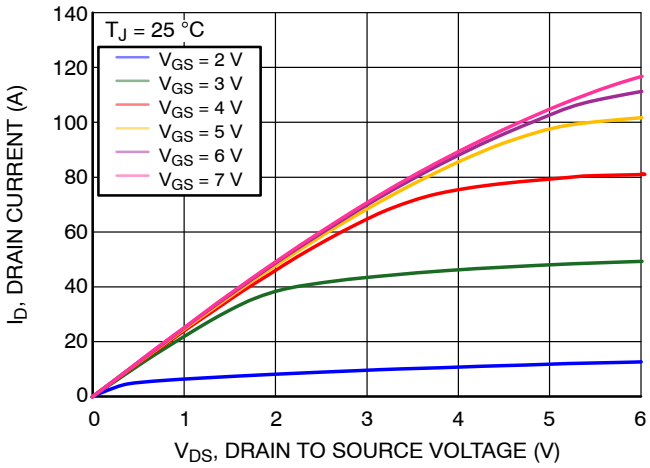


**Figure 1. Output Characteristics at $T_J$ = 25 °C**

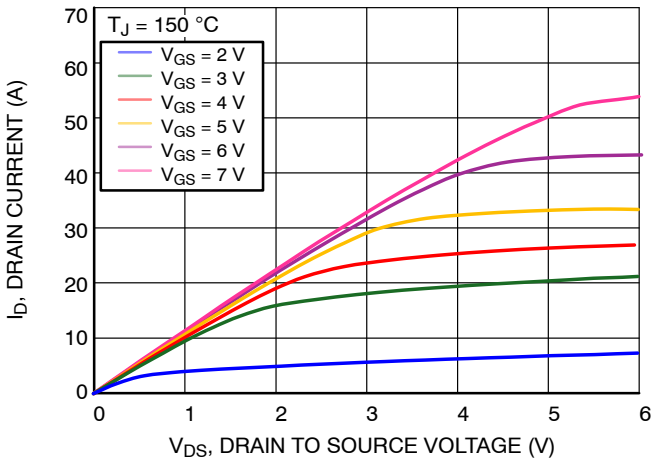


**Figure 2. Output Characteristics at $T_J$ = 125 °C**

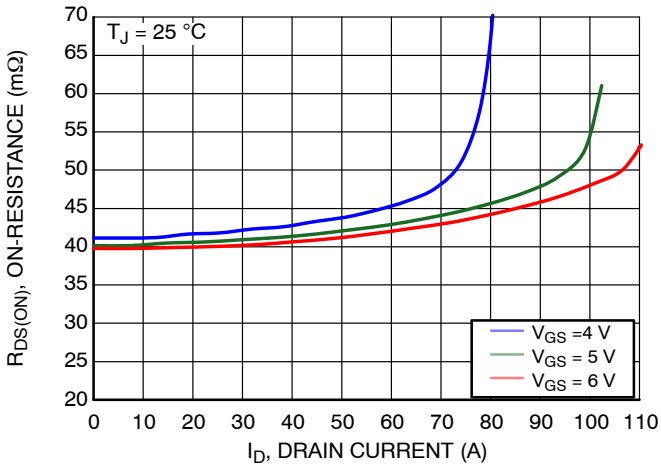


**Figure 3. On-Resistance vs. Drain Current at $T_J$ = 25 °C**

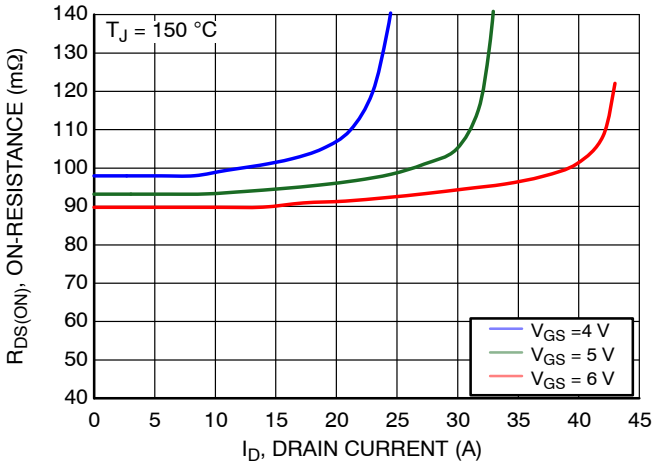


**Figure 4. On-Resistance vs. Drain Current at $T_J$ = 125 °C**

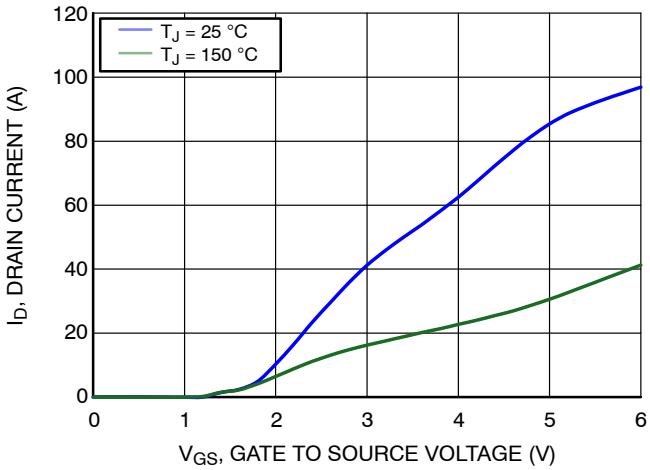


**Figure 5. Transfer Characteristics at $V_{DS}$ = 3 V**

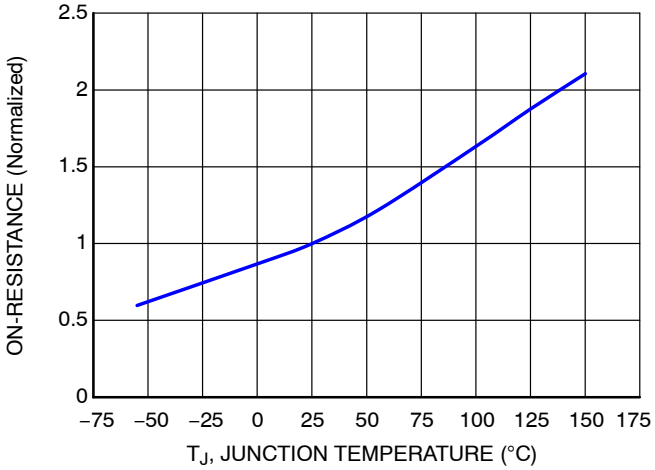


**Figure 6. Normalized On-Resistance vs. Temperature at $V_{GS}$ = 6 V**



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## TYPICAL CHARACTERISTICS ($T_J$ = 25 °C unless otherwise specified)

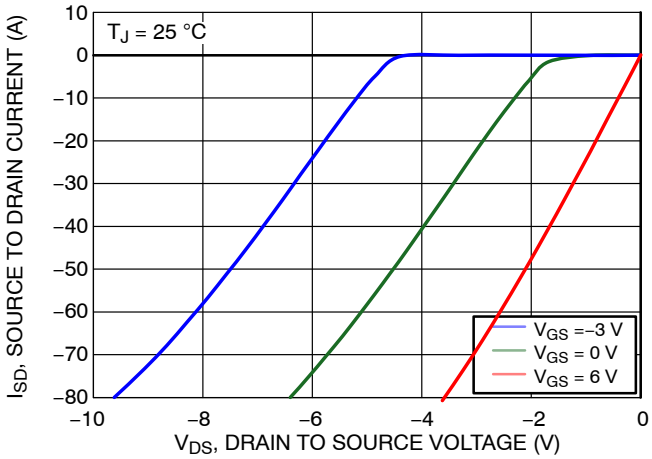


**Figure 7. Reverse Conduction Characteristics at $T_J$ = 25 °C**

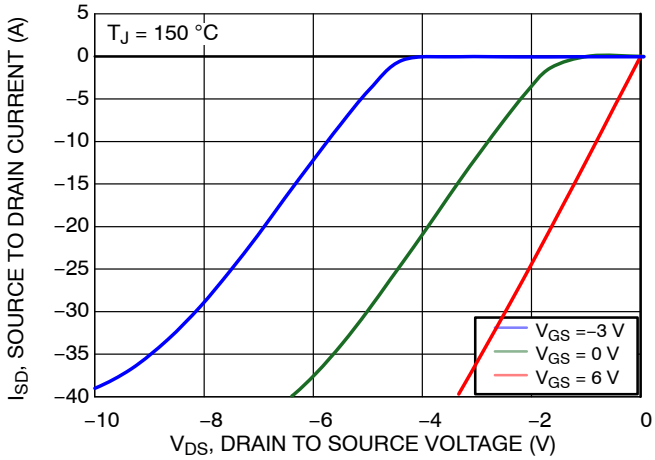


**Figure 8. Reverse Conduction Characteristics at $T_J$ = 125 °C**

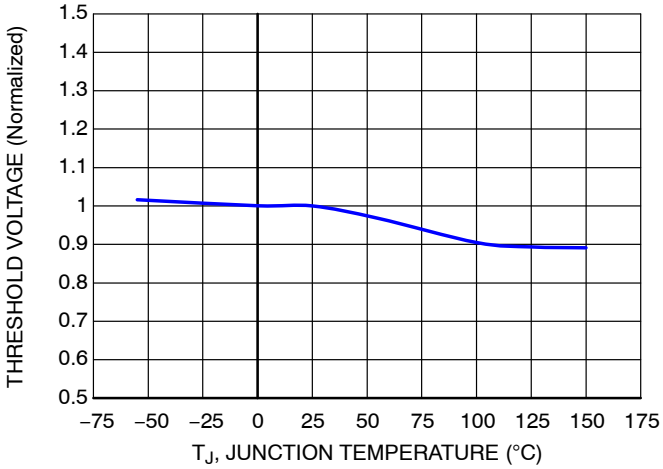


**Figure 9. Normalized Threshold Voltage vs. Temperature**

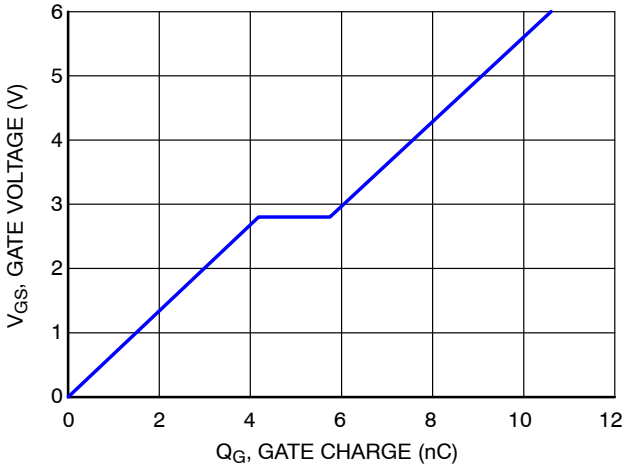


**Figure 10. Gate Charge Characteristics at $I_{DS}$ = 13 A**

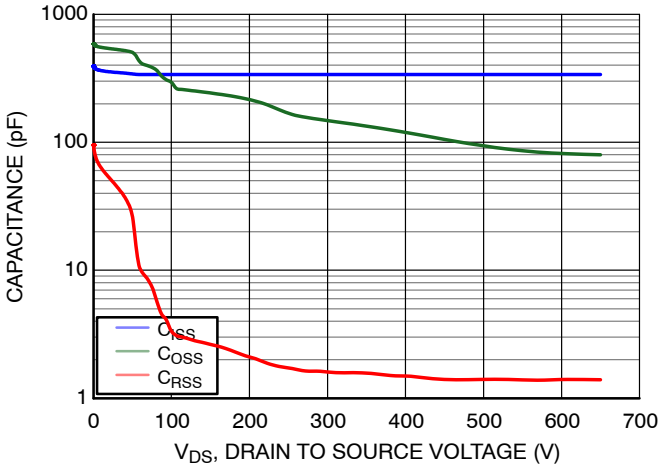


**Figure 11. Capacitance Characteristics**

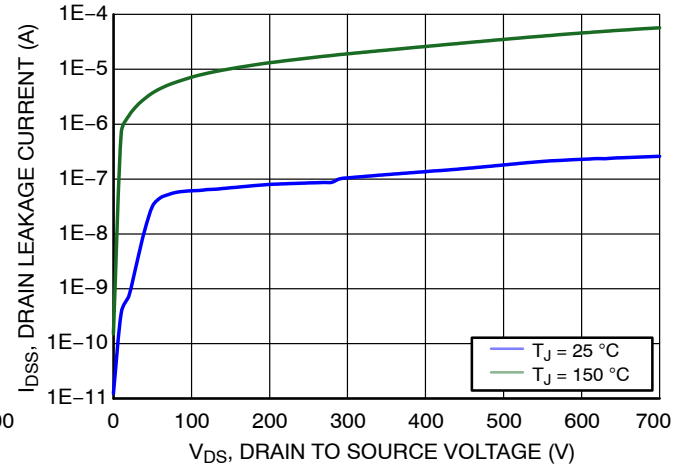


**Figure 12. Drain Leakage Characteristics**



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## TYPICAL CHARACTERISTICS ($T_J$ = 25 °C unless otherwise noted)

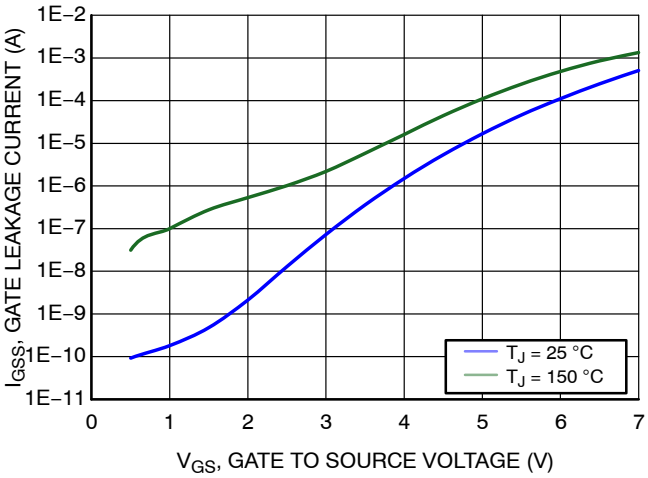


**Figure 13. Gate Leakage Characteristics**

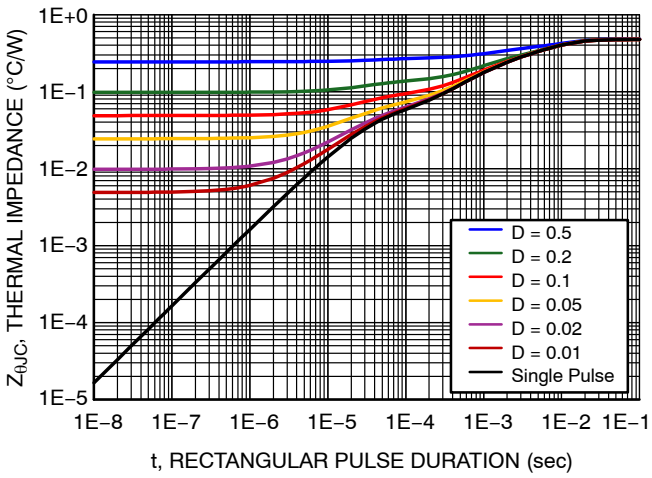


**Figure 14. Transient Thermal Impedance**

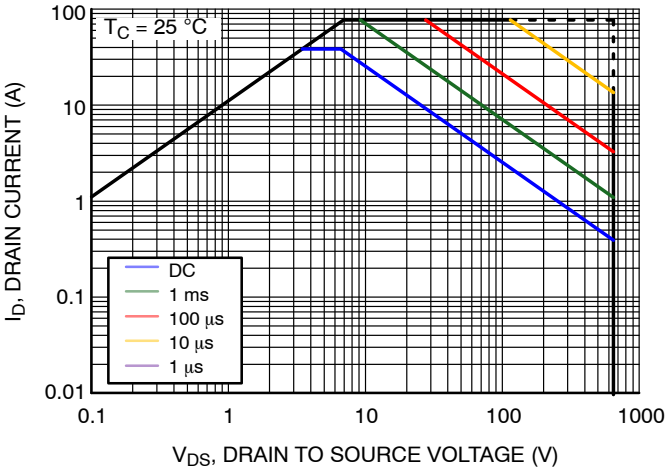


**Figure 15. Safe Operating Area at $T_C$ = 25 °C**

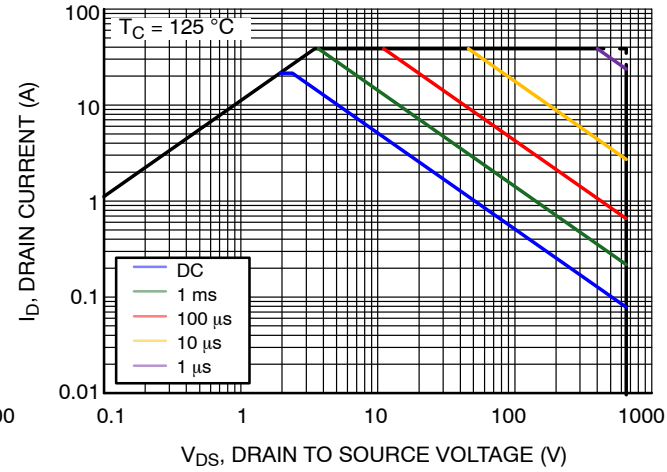


**Figure 16. Safe Operating Area at $T_C$ = 125 °C**



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**Gate Drive Guidelines**

This GaN device utilizes a Schottky gate structure, which behaves similarly to a MOSFET with a purely capacitive input and does not require continuous gate current during the on-state. For optimal performance, apply a low-impedance gate driver with appropriate gate resistance to control switching speed and limit ringing. A typical gate voltage of **6 V** is recommended, with optional negative gate bias for hard-switching applications to improve dv/dt immunity and prevent false turn-on. Minimize gate loop inductance (<1 nH) through careful PCB layout and short connections. For additional robustness, Zener clamps may be used to limit gate voltage in both polarities.

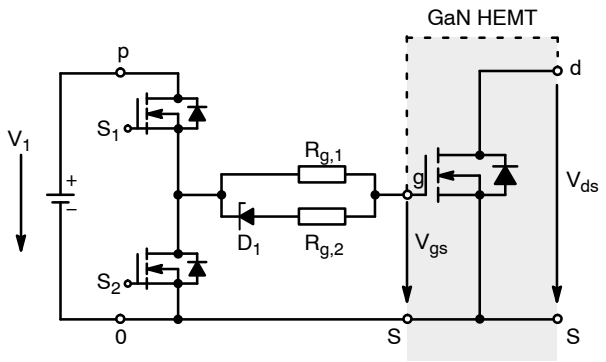


**Figure 17. Schottky Gate Conventional Driver Schematic**

**ORDERING INFORMATION**

| Device Order Number | Package Type | Shipping† |
|---|---|---|
| NTBL050N65GN1TXG | PDSO-F9 10.38 x 9.90 x 2.30, 1.20P | 1200 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 0 | Initial document release. | 7/29/2026 |



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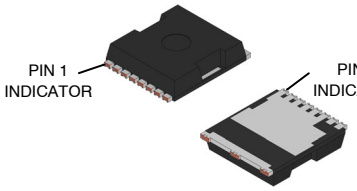
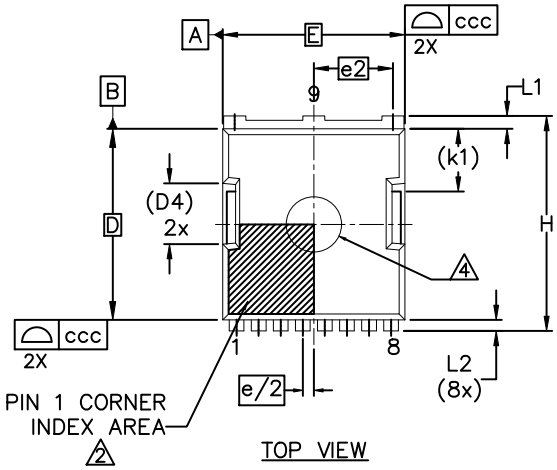
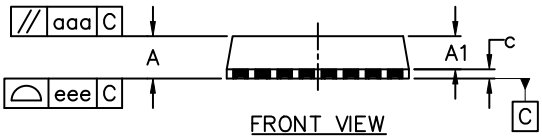
**PDSO-F9 10.38x9.90x2.30, 1.20P**
CASE 207AA
ISSUE O

DATE 25 FEB 2026

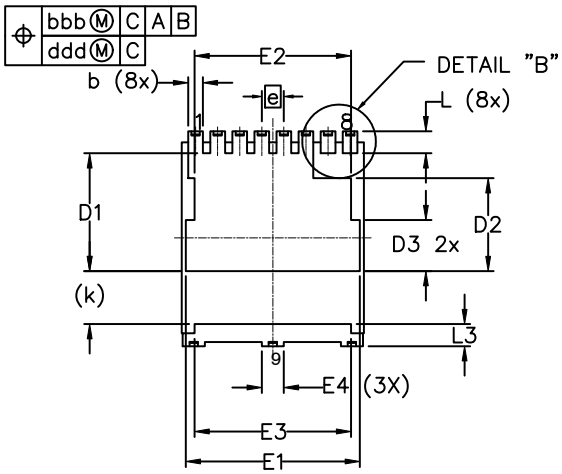


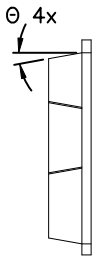

TOP VIEW



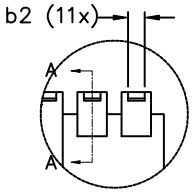

FRONT VIEW



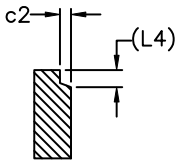

BOTTOM VIEW




SIDE VIEW




DETAIL "B"
SCALE: 2X




SECTION "A–A"
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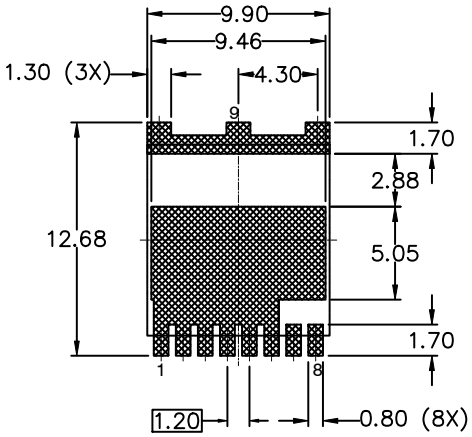
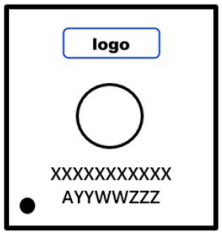



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 2.15 | 2.30 | 2.45 |
| A1 | 1.65 | 1.80 | 1.95 |
| b | 0.70 | 0.80 | 0.90 |
| b2 | 0.31 | 0.43 | 0.55 |
| c | 0.40 | 0.50 | 0.60 |
| c2 | 0.10 | – | – |
| D | 10.38 BSC | | |
| D1 | 6.20 | 6.40 | 6.60 |
| D2 | 4.85 | 5.05 | 5.25 |
| D3 | 2.57 | 2.77 | 3.97 |
| D4 | 3.30 REF | | |
| E | 9.90 BSC | | |
| E1 | 9.26 | 9.46 | 9.66 |
| E2 | 8.30 | 8.50 | 8.70 |
| E3 | 8.30 | 8.50 | 8.70 |
| E4 | 1.10 | 1.20 | 1.30 |
| e | 1.20 BSC | | |
| e/2 | 0.60 BSC | | |
| e2 | 4.30 BSC | | |
| H | 11.48 | 11.68 | 11.88 |
| L | 1.00 | 1.20 | 1.40 |
| L1 | 0.50 | 0.70 | 0.90 |
| L2 | 0.50 | 0.60 | 0.70 |
| L3 | 1.00 | 1.20 | 1.40 |
| L4 | 0.23 REF | | |
| k | 2.88 REF | | |
| k1 | 3.41 REF | | |
| Θ | 10° REF | | |
| aaa | 0.20 | | |
| bbb | 0.25 | | |
| ccc | 0.20 | | |
| ddd | 0.20 | | |
| eee | 0.20 | | |

**GENERIC MARKING DIAGRAM***




XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH AND BURR.
4. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.

| DOCUMENT NUMBER: | 98AON70698H | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | PDSO-F9 10.38x9.90x2.30, 1.20P | PAGE 1 OF 1 |

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