MOSFET - Power, Single N-Channel, DUAL COOL®, TDFNW8

80 V, 0.90 mΩ, 396 A

NTMTSC0D9N08X

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	0.90 mΩ @ V_{GS} = 10 V	396 A

Features

- Advanced Dual-Side Cool Package
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Supply Unit (PSU)
- Battery Management System Protection
- Motor Drive
- Synchronous Rectifier
- ORing

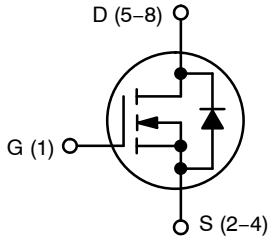
MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

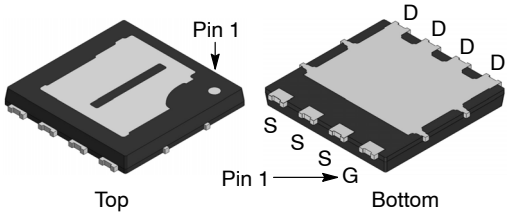
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	396	A
	T_C = 100 °C		280	
Power Dissipation	T_C = 25 °C	P_D	283	W
Pulsed Drain Current	T_C = 25 °C, t_p = 100 μs	I_{DM}	2388	A
		I_{SM}		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Source-Drain Current (Body Diode)	T_C = 25 °C	I_S	283	A
Single Pulse Avalanche Energy (I_{PK} = 110 A)		E_{AS}	605	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in^2, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} is based on started T_J = 25 °C, rated I_{AS}, V_{DD} = 64 V, V_{GS} = 10 V, 100% avalanche tested.

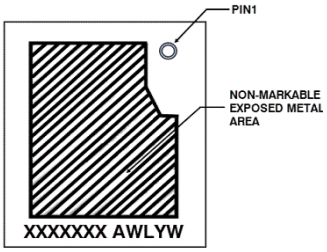
N-CHANNEL MOSFET





TDFNW8
CASE 507AS

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case (Bottom)	$R_{\theta JCB}$	0.53	°C/W
Thermal Resistance, Junction-to-Case (Top)	$R_{\theta JCT}$	0.58	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	30	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25 °C		20		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25 °C			10	μA
		V_{DS} = 80 V, T_J = 125 °C (Note 4)			250	
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 32 A, T_J = 25 °C		0.76	0.90	mΩ
		V_{GS} = 6 V, I_D = 32 A, T_J = 25 °C		1.2	1.5	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 580 μA, T_J = 25 °C	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 580 μA		−7.5		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 30 A		164		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance (Note 4)	C_{ISS}	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	5234	10468	15702	pF
Output Capacitance (Note 4)	C_{OSS}			3016	4524	
Reverse Transfer Capacitance (Note 4)	C_{RSS}			45	90	
Output Charge	Q_{OSS}			216		nC
Total Gate Charge (Note 4)	$Q_{G(TOT)}$	V_{DD} = 40 V, I_D = 32 A, V_{GS} = 6 V		90	135	
		V_{DD} = 40 V, I_D = 32 A, V_{GS} = 10 V		146	219	
Threshold Gate Charge	$Q_{G(TH)}$			32		
Gate-to-Source Charge	Q_{GS}			46		
Gate-to-Drain Charge (Note 4)	Q_{GD}			23	46	
Gate Plateau Voltage	V_{GP}			4.4		V
Gate Resistance (Note 4)	R_G	f = 1 MHz	0.25	0.50	0.75	Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 40 V, I_D = 32 A, R_G = 2.5 Ω		45		ns
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(OFF)}$			72		
Fall Time	t_f			12		
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 32 A, T_J = 25 °C		0.78	0.93	V
		V_{GS} = 0 V, I_S = 32 A, T_J = 125 °C		0.61		

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 32 A, dI/dt = 1000 A/μs, V_{DD} = 40 V, T_J = 25 °C		36		ns
Charge Time	t_a			20		
Discharge Time	t_b			16		
Reverse Recovery Charge	Q_{RR}			345		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Defined by design, not subject to production test.

TYPICAL CHARACTERISTICS

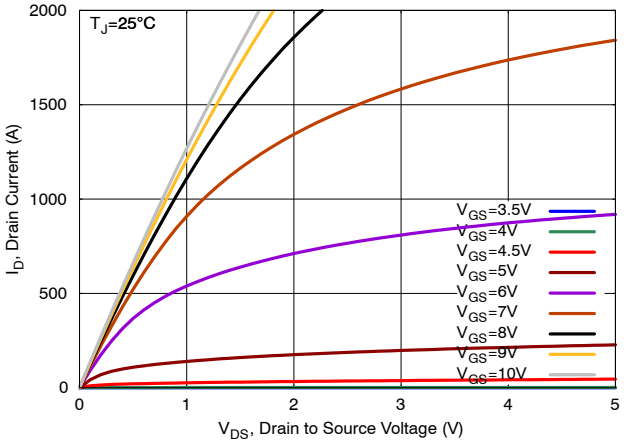

Figure 1. On−Region Characteristics

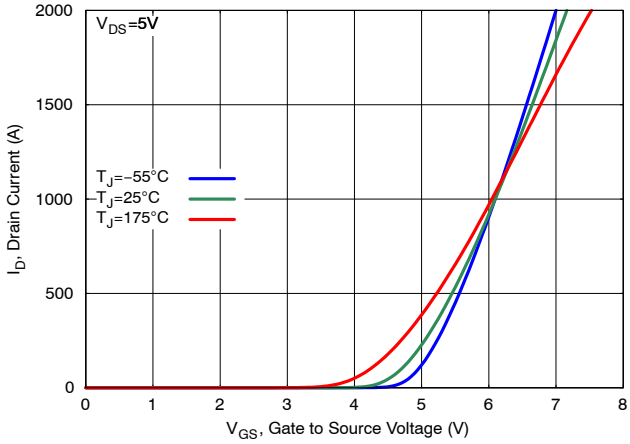

Figure 2. Transfer Characteristics

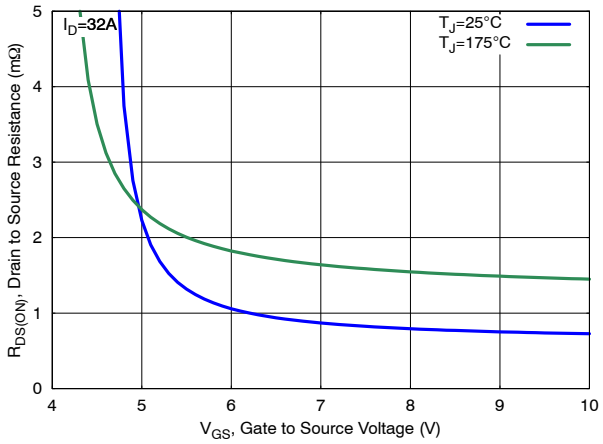

Figure 3. On−Resistance vs. Gate Voltage

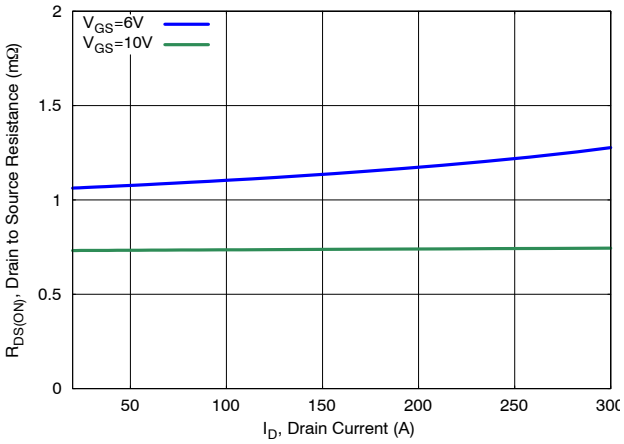

Figure 4. On−Resistance vs. Drain Current

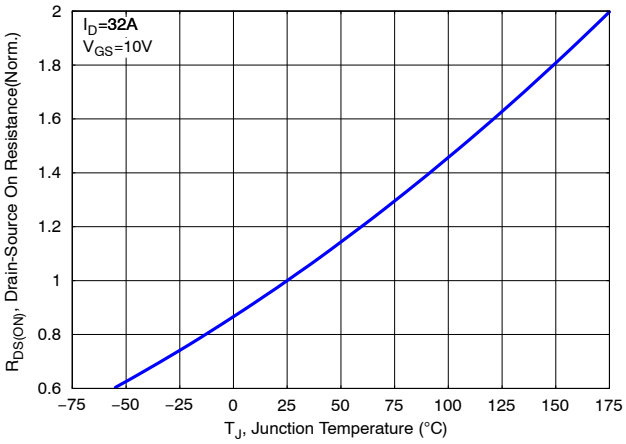

Figure 5. Normalized ON Resistance vs. Junction Temperature

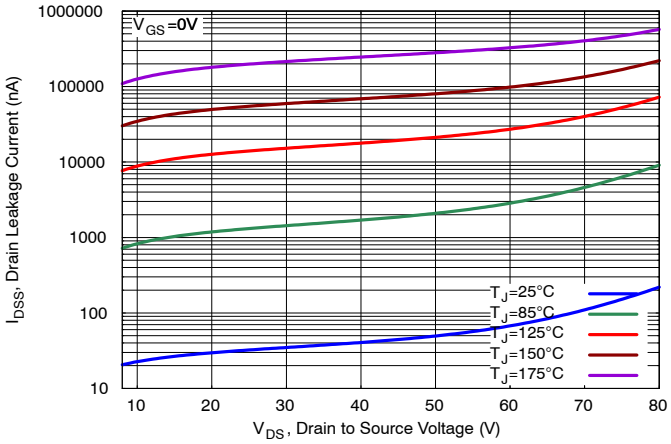

Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS (continued)

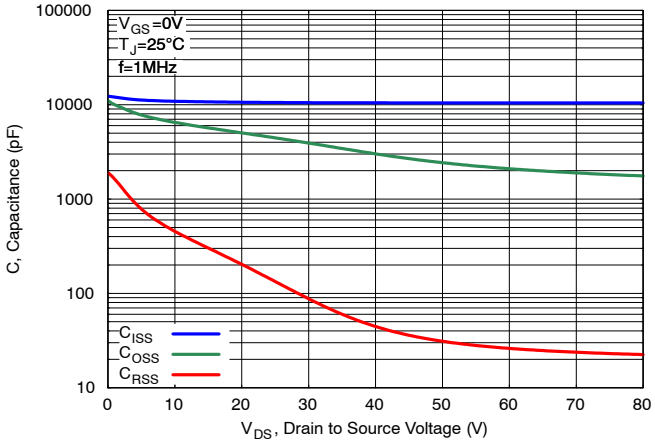

Figure 7. Capacitance Characteristics

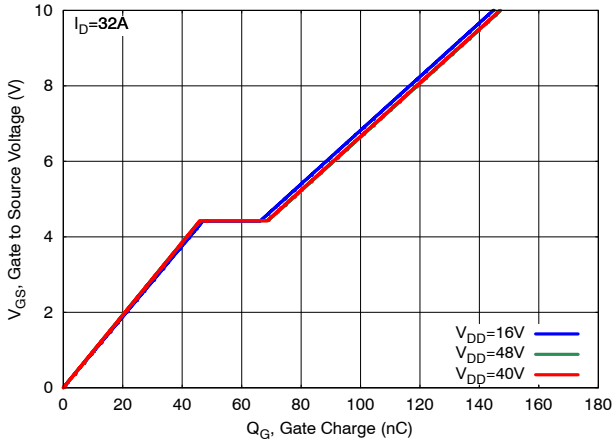

Figure 8. Gate Charge Characteristics

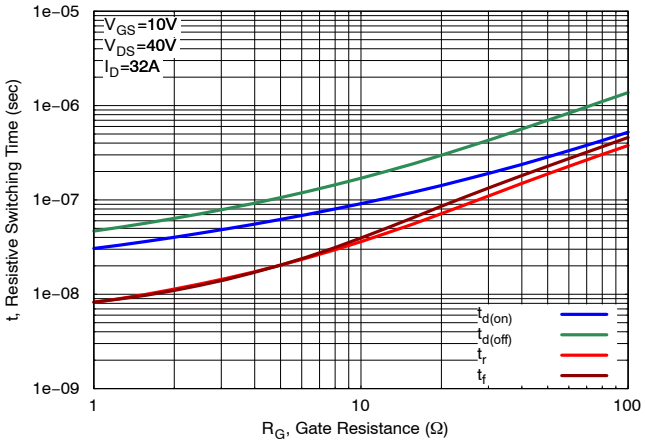

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

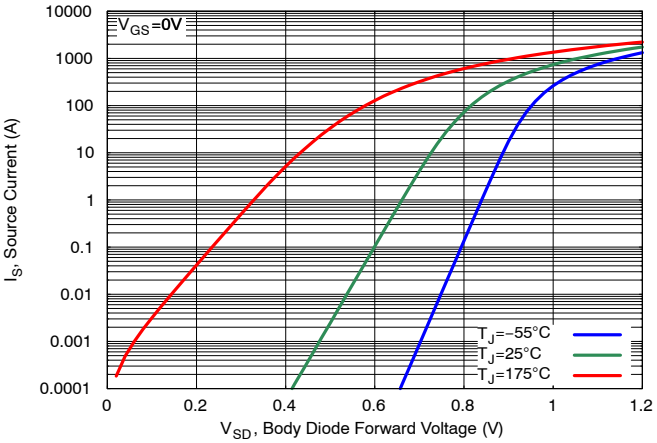

Figure 10. Diode Forward Characteristics

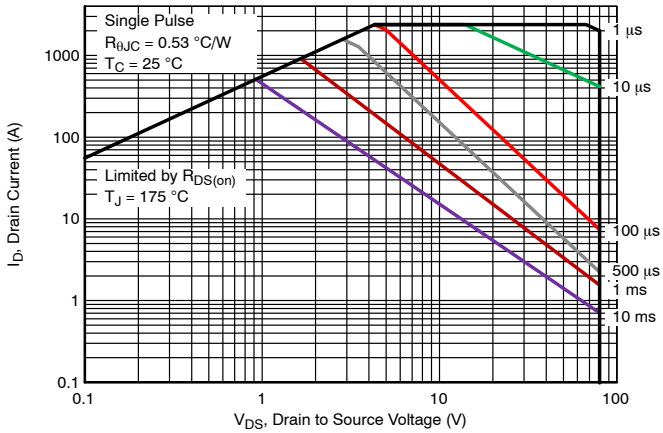

Figure 11. Safe Operating Area (SOA)

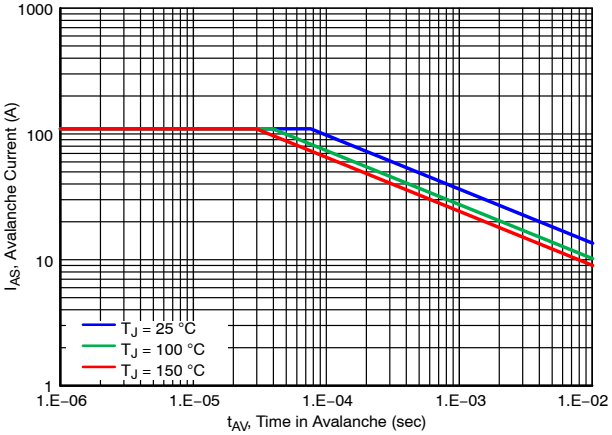

Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS (continued)

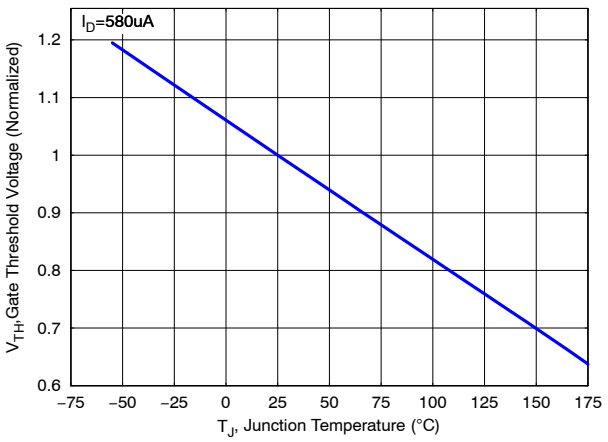

Figure 13. Gate Threshold Voltage vs. Junction Temperature

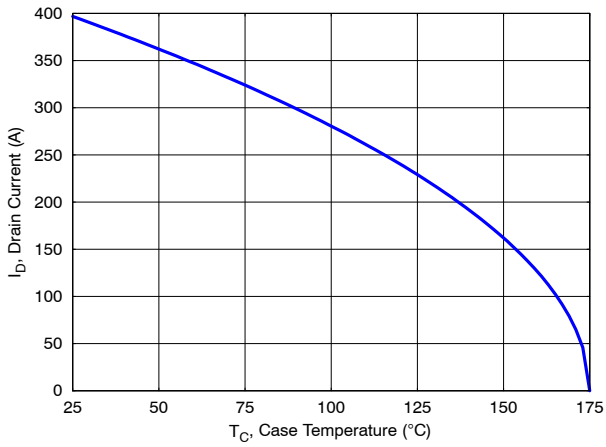

Figure 14. Maximum Current vs. Case Temperature

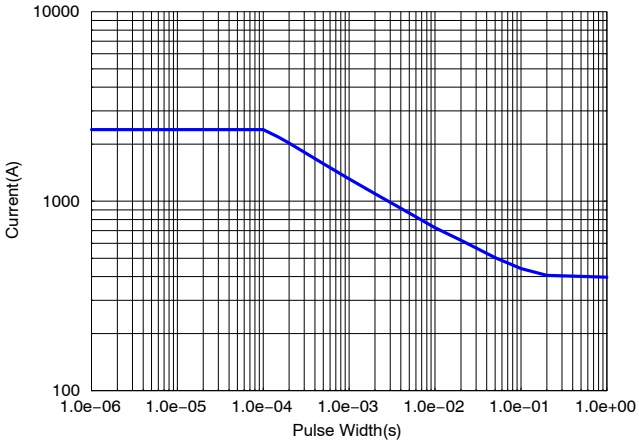

Figure 15. IDM vs Pulse Width

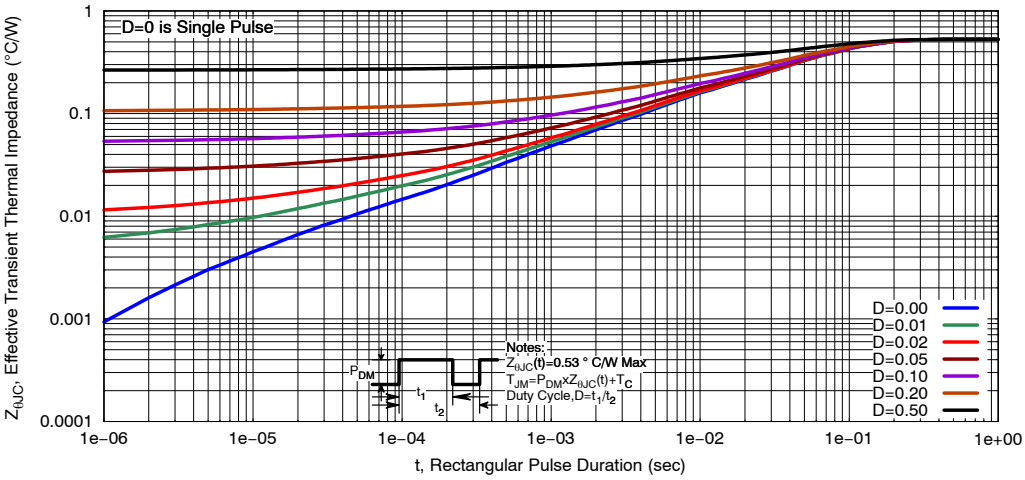

Figure 16. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMTSC0D9N08XTXG	0D9N08X	TDFNW8	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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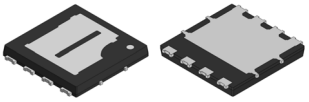
REVISION HISTORY

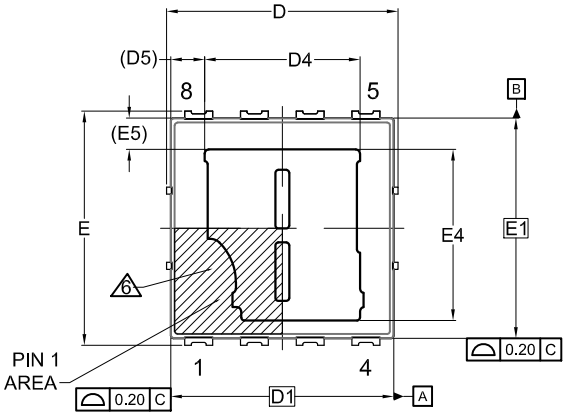
Revision	Description of Changes	Date
0	Initial document release.	7/17/2026

PACKAGE DIMENSIONS

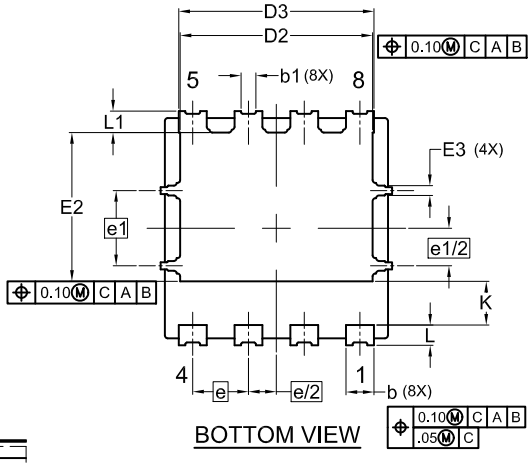


TDFNW8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE C

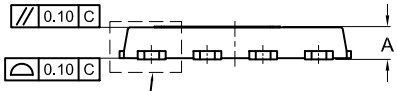
DATE 28 MAY 2024



TOP VIEW

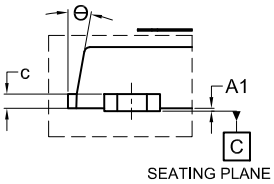


BOTTOM VIEW



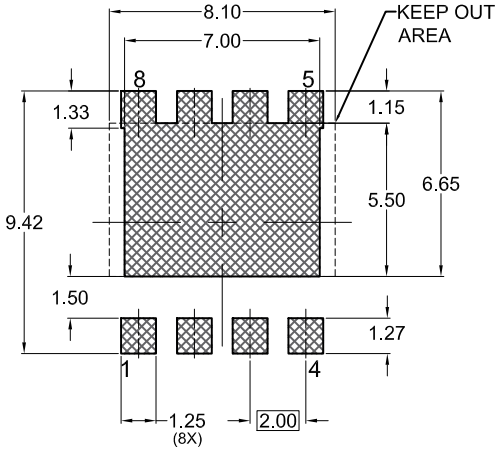
SEE DETAIL A

FRONT VIEW



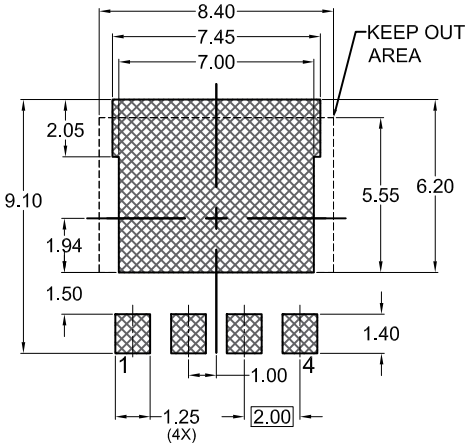
DETAIL A
(SCALE: 2X)

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. SLOT PARTITION IS OPTIONAL.



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.



UNIVERSAL LAND PATTERN*

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	—	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	8.00 BSC		
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	5.52	5.67	5.82
D5	1.16 REF		
E	8.30	8.40	8.50
E1	7.90 BSC		
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	6.08	6.23	6.38
E5	1.13 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	—	12°

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